Design and Implementation of High- performance MAC Unit

Shishir Kumar Das, Aniruddha Kanhe, R.H. Talwekar

Abstract—In real-life, embedded devices like mobile phone, notebook computers are made use of RISC processor and DSP .In Digital Signal Processing (DSP) applications the critical operations usually involve many multiplications and/or accumulations. So, for real time signal processing, the high speed multiplier accumulator (MAC) unit is always a key element to achieve a high-performance digital signal processing. The goal of this project is to design and implement the MAC unit for high-speed DSP applications. For designing the MAC unit various multipliers and adders are required. The MAC unit is implemented using VHDL, synthesized and simulated using Xilinx ISE 12.1.

Keywords—: Adders, CAD tools, multipliers, VHDL.

1 INTRODUCTION

IN the majority of the Digital signal processing (DSP) applications the critical operations usually involve many multiplications and accumulations. So, for real time signal processing applications high throughput multiplier accumulator (MAC) is always a key element to achieve a high-performance digital signal processing. In the last few years, the main consideration of MAC design is to enhance its speed. This is because speed and throughput rate are always the concern of digital signal processing systems. Due to the increase of portable electronic products, low power designs also become major considerations. This is because the limited battery energy of these portable products restricts the power consumption of the system.The main motive is to investigate various MAC architectures and the design techniques which are suitable for the implementation of high throughput signal processing units.

The goal of this project is to design and implement Low power and high speed MAC unit. The total process is coded in VHDL. Finally, the whole process is implemented on Virtex 5 FPGA. The paper is organized as follows: Section 2 presents the overview of MAC unit. The implementation of MAC unit using carry select Adder and Vedic Multiplier is discussed in Section 3. The implementation results are given in section 4, followed by conclusion in section 5.

2 OVERVIEW OF MAC UNIT

A basic MAC unit consists of an adder, multiplier and an accumulator. Usually, adders implemented are Carry-Select or Carry-Save adders, as speed is of utmost importance in DSP.

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But if on chip area is to be considered then, Carry increment Adder can be used with an additional advantage of high speed [1]. One implementation of the multiplier could be Vedic Multiplier [2].

2.1 Operation of MAC Unit

The inputs of MAC unit are fetched from memory cell and fed to the multiplier block of the MAC, which will perform multiplication and give the result to adder and then store the result in to a memory location. This entire process is to be achieved in a single clock cycle.

The proposed design consists of 32-bit floating point multiplier based on Vedic multiplication technique, 65-bit accumulator using carry select adder. To multiply the values of A and B, Floating point Vedic multiplier is used instead of conventional multiplier because Vedic multiplier can increase the speed of MAC unit. Carry select adder is used as an accumulator in this design. Apparently, together with the utilization of Vedic multiplier approach, Carry select adder as the accumulator,

This MAC unit design is not only reducing the standby power consumption but also can enhance the MAC unit speed so as to gain better system performance.

3 DESIGN OF MAC UNIT

The Fig.1 shows the block diagram of proposed MAC Unit consisting of 32 bit IEEE 754 based floating point Vedic Multiplier unit.The result of multiplier is provided to the input of Accumalotor through Carry select adder.

3.1 Multiplier Unit

In the proposed design of MAC Unit the Multiplier used is a 32 BIT IEEE 754 floating point multiplier based on Vedic multiplication technique. The multiplier for the floating point numbers represented in IEEE 754 format [3] can be divided in four sections: Mantissa Calculation Unit, Exponent Calculation Unit, Sign Calculation Unit, and Control Unit [4].

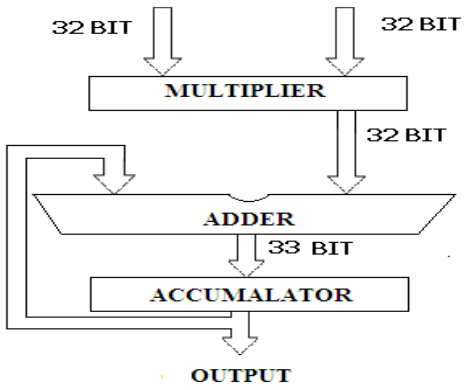

Fig. 1. Block Diagram of Proposed MAC Unit

The Vedic Multiplication technique is chosen for the implementation of this unit. This technique gives promising result in terms of speed and power [2,4].The Vedic multiplication system is based on 16 Vedic sutras or aphorisms, which describes natural ways of solving a whole range of mathematical problems. Out of these 16 Vedic Sutras the Urdhvatriyakbhyam sutra is suitable for this purpose. In this method the partial products are generated simultaneously which itself reduces delay and makes this method fast. The method for multiplication of two, 3 BITs number is shown Fig.2.

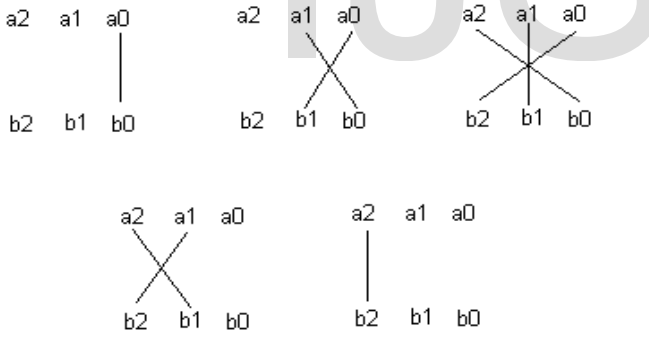

Fig.2 Vedic multiplication Method

Consider the numbers A and B where A = a2a1a0 and B = b2b1b0. The LSB of A is multiplied with the LSB of B:
s0=a0b0;
Then a0 is multiplied with b1, and b0 is multiplied with a1
And the result added together as:
c1s1=a1b0+a0b1;
Here c1 is carry and s1 is sum. Next step is to add c1 with the multiplication results of a0 with b2, a1 with b1 and a2 with b0.
c2s2=c1+a2b0+a1b1 + a0b2;
Next step is to add c3 with the multiplication results of a1 with b2 and a2 with b1.
c3s3=c2+a1b2+a2b1;
Similarly the last step
c4s4=c3+a2b2;
Now the final result of multiplication of A and B is c4s4s3s2s1s0.

3.2 Adder Unit

A carry-select adder is divided into sectors, each of which – except for the least-significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one. A four bit carry select adder generally consists of two ripple carry adders and a multiplexer. The carry-select adder is simple but rather fast. Adding two n-bit numbers with a carry select adder is done with two adders (two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correctcarry is known.A carry-select adder speeds 40% to 90%faster than RCA by performing additions in parallel and reducing the maximum carry path.

4 RESULT

We are evaluating the performance of the high speed low power MAC Unit implemented using, 32 bit IEEE 754 Floating point multiplier based on Vedic Multiplication technique. The Table.1 shows the simulation result of Vedic multiplier and also comparision between conventional Array Multiplier aswellas Booth Multiplier. These multipliers are implemented using VHDL In order to get the power and delay report the multipliers are synthesized using Xilinx ISE tool and Spartan 2E FPGA is used. Table 1 compares the simulation result of multipliers with Vedic Multiplier on basis of time delay and power.

Table1. Comparison between multipliers

Multiplier Type	FPGA Type	Delay ns	Power Dissipation mW
Array Multiplier [6]	Spartan 2	14.886	40
Booth Multiplier	Spartan 2	15.092	35
Vedic Multiplier	Spartan 2	6.801	31

The Floating point multiplier Unit of proposed MAC is designed in VHDL and simulated using Modelsim Simulator. The design was synthesized using Xilinx ISE 12.1 tool targeting the Xilinx Virtex 5 Xc5vlx30-3-ff324 FPGA. The paper shows the efficient use of Vedic multiplication method to multiply two floating point numbers. The lesser number of LUTs verifies that the hardware requirement is reduced, thereby reducing the power consumption. The power is reduced affectively still not compromising delay so much. The Table 2 shows simulation result of floating point multiplier [5].

Table2. Design Summary

Parameters	This work	[7]
Device	Virtex 5 FPGA	Virtex 2p
Time delay	5.246ns	3.070ns
Number of LUTs	966	1316
Number of IOs	99	100
Total dynamic power	27.29mW	55mW

5 CONCLUSION

The propose design shows the efficient use of Floating point Multiplier for implemtation of MAC Unit. As the hardware requirement of porposed Multiplier unit is less and also the dynamic power dissption.Hence can be used for implementation of high performance MAC Unit.

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